New Hybrid-Based Self-Test Strategy for Faulty Modules of Complex Microcontroller Systems

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Abstract

have become a widely accepted architecture for highly complex embedded systems on a single chip (SoC). It consists of deeply embedded heterogeneous components with poor accessibility makes their testing process a difficult task using hardware based self-test (HBST). Software-based self-test (SBST) is considered to be a promising testing technology for these systems. Almost every SoC contains at least one embedded processor, SBST utilize this processor for test pattern generation (TPG) and test response compaction (TRC) based on its instruction set, then test response will be unloaded and evaluated using external automatic test equipment (ATE). In this paper, SBST strategy disadvantages in microcontroller testing will be identified. Then, a new testing approach that combines both the HBST and the SBST, called hybrid-based self-test (HYBST) will be introduced. Based on a divide-and-conquer approach, HYBST identify microcontroller's components and their corresponding component operations. Feasibility and effectiveness of HYBST and SBST methodologies will be assessed by applying them to a Microchip È PIC16F877A and PIC18F452 in terms of memory usage, time consumption and number of tested modules found in microcontrollers.

Electronics Journal (Publisher:Faculty of Electrical Engineering Banja Luka. 2018, December

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