Test Pattern Generator Optimization for Digital Testing of Analogue Circuits

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Abstract

In this paper, the proposed design for digital testing of analogue circuits (DTAC) is presented. The proper selection of the analogue test pattern generator (ATPG) for stimulating and detecting faults is the target issue. Component tolerance of the analogue circuit under test produces signature boundaries in the analogue test response compactor. Signature boundary difference (SBD) is determined for different ATPGs. The minimization of the SBD increases the differentiation between the faulty and golden cases. Each part of the DTAC is modeled and evaluated to select the proper ATPG such that the SBD is minimized. Based on the experimental results of some analogue benchmark circuits, the best ATPG for detecting faults is selected based on the minimal SBD. Different ATPGs may change from a circuit to another one. These results are contrary to the previous published work that selected the pulse waveform as the best ATPG because of its superiority in terms of power spectral density.

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