

Design and FPGA implementation of novel adaptive post detection integration algorithm

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Abstract

In the present work, design and Field Programmable Gate Array (FPGA) implementation of a new Adaptive Post detection Integration (API) algorithm, designated as Conditioned Adaptive Post detection Integration (C-API), is proposed. The proposed C-API algorithm overcomes the problem of azimuth resolution degradation in the traditional API, especially for high signal to noise ratios (SNRs), and gives a robust performance against asynchronous pulse interference without affecting the detection capability of the traditional API. Computer simulations and experimental measurements are provided to validate the superiority of the proposed C-API algorithm against the traditional API and the Adaptive Binary Integrator (ABI).

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