Efficient Microcontroller System to Test an SRAM Chip Using Signature Analysis

Mohamed Hassan Elmahlawy ,Mahmoud S. Ragab ; Emad A. El-Samahy

Abstract

Memory in recent technology is considered an important element in the electronic system. It is required to test the memory for high fault coverage and less test application time. In this paper, the low-cost design of the microcomputer-based testing (MBT) for the static random access memory (SRAM) is presented using signature analysis. The memory test pattern generator (MTPG), the test response compaction based on the signature analysis, the memory under test (MUT), and the memory test controller are considered the main parts of the MBT. The proper selection of the MTPG for stimulating and detecting faults is the target issue. In this paper, all March tests that detect memory faults are considered. The combination of March tests is selected to select the proper MTPG and to detect all current faults of the MUT. Using UD- and LSD March tests with test sequence length, 87n, all possible current memory faults based the MBT are detected.

13th International Computer Engineering Conference (ICENCO), Dec 27-28, 2017 2017, December

Future University In Egypt (http://www.fue.edu.eg)

Copyright É 2026 [Future University in Egypt]. All rights reserved.