FPGA-Based Implementation of the Digital Testing of Analogue Circuits

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Abstract

This paper presents a new parametric fault detection testing approach for analogue circuits, based on digital testing. The design and implementation is achieved using the field programmable gate array (FPGA) as the digital part besides the analogue part that includes the analogue conditioning and the data acquisition circuitry. The analogue test pattern generator (ATPG) is designed to sweep frequencies of the sinusoidal waveform to match the frequency domain of the analogue circuit under test (ACUT). The binary generation of the ATPG can be viewed as variable delay samples of the swept sinusoidal signal. The analogue test response compactor (ATRC) is designed based on sample accumulation of the test response to generate a digital signature. The test controller is designed to enable the proper synchronization of the analogue test cycle for stable digital signature generation. The signature comparison is achieved based on signature boundary of the worst-case analysis. In addition, the deduced signature combines effective parameters of the transfer function of the ACUT with respect to the component variations. These parameters are the bandwidth (BW) and the pass-band transmission (Amax). Then, the signature curve of each component variations in the ACUT is used for the ACUT judgment. The presented analogue testing is applied to the ACUT, selected from the analogue benchmark circuits in the frequency range of biomedical applications.

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