Low-Power Low-Noise CTIA Readout Integrated Circuit Design for Thermal Imaging Applications

Mohamed Hassan Elmahlawy ,Mohmed Raffat, Ahmad Hafez, and Mahmoud S. Hamed

Abstract

This paper targets the design of a high dynamic range low-power, low-noise pixel readout integrated circuit (ROIC) that handles the infrared (IR) detectorôs output signal of the uncooled thermal IR camera. Throughout the paper, both the optics and the IR detector modules of the IR camera are modeled using the analogue hardware description language (AHDL) to enable extracting the proper input signal required for the ROIC design. A capacitive trans-impedance amplifier (CTIA) is selected for design as a column level ROIC. The core of the CTIA is designed for minimum power consumption by operation in the sub-threshold region. In addition, a design of correlated double sampling (CDS) technique is applied to the CTIA to minimize the noise and the offset levels. The presented CTIA design achieves a power consumption of 5.2εW and root mean square (RMS) output noise of 6.9εV. All the circuits were implemented in 0.13Õm CMOS process technology. The design rule check (DRC), layout versus schematic (LVS), parasitic extraction (PE), Process-voltage-temperature (PVT) analysis and post-layout simulation are performed for all designed circuits. The post-layout simulation results illustrate enhancement of the power consumption and noise performance compared to other published ROIC designs. Finally, a new widening dynamic range (WDR) technique is applied to the CTIA with the CDS circuit designs to increase the dynamic range (DR).

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