# Parametric Fault Detection of Analogue Circuits

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**Abstract**

This paper presents a new testing approach for analogue circuits based on the digital signature analysis. In this paper, the efficient parametric fault detection approach for analogue circuits using the simulation environment is presented. This approach has three main parts, an analogue test pattern generator (ATPG), an analogue test response compactor (ATRC), and an analogue circuit under test (ACUT) model, build in the PSpice circuit simulator. The proper ATPG is designed to sweep the applying sinusoidal frequencies to match the frequency domain of the ACUT. The output test response of the ACUT is acquired via the analogue-to-digital converter (ADC). The ATRC accumulates digital samples of the output response from the ADC to generate a digital signature that can characterize the situation of the ACUT. The signature comparison is achieved based on signature boundaries based on the worst-case analysis. In addition, the signature curve for each component variations of the ACUT is presented to be illustrated as image of some parameters affected in the transfer function of the ACUT. It combines effective parameters of the transfer function of the ACUT with respect to the component variations. These parameters are the band-with and the passband transmission. Using the signature curve, a parametric fault of each component of the ACUT can be detected under the sweep sinusoidal frequency of the ATPG. The presented testing approach is applied to the analogue benchmark circuit to validate the presented testing approach.

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