Signature Multi-Mode Hardware-Based Self-Test Architecture for Digital Integrated Circuits

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Abstract

In this paper, the new signature multi-mode hardware-based self-test architecture (SM-HBST) for digital integrated circuits (ICs) is presented for fault diagnosis. It generates test patterns either pseudo-randomly, or deterministically to test the random logic. Also, it generates efficient test patterns to test the static random access memory (SRAM) based on March testing approach. The response of the circuit is evaluated by the test response compactor (TRC). The proper timing between the test pattern generator (TPG), the circuit under test (CUT), and the TRC is achieved to control the test cycle for stable signature generation. In addition, this architecture can test the single-shot (SS) circuit by measuring the time duration based on the edge detecting of the generated pulse. This time duration is considered the signature of its proper functionality. The SM-HBST is design and implemented based on the Field Programmable Gate Array (FPGA) technology. The experimental results illustrate the efficiency of the SM-HBST as the integrated test solution for fault diagnosis of the digital circuit boards.

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