Two-Test Pattern Capabilities of the LFSR/SR Generator in Pseudo-Exhaustive Testing based on Coding Theory Principles

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Abstract

Testing of digital integrated circuits for delay and CMOS stuck-open faults requires two-test patterns. Built-in self-test (BIST) schemes are required to comprehensive testing of such faults. BIST test pattern generators for two-test pattern should be designed to ensure high transition coverage. The test pattern generator (TPG) circuits treated here are not limited to linear feedback shift registers (LFSRs) but include the linear feedback shift register / shift register (LFSR/SR) circuits. It is required to increase the number of each subset of the state variables for complete transition coverage based on the optimal test lengths. In this paper, the two-test pattern capabilities of the LFSR/SRs are explored using transition coverage as the metric. The necessary and sufficient conditions to ensure complete transition coverage for LFSR/SRs are derived. The theory, developed here, identifies all LFSR/SRs as the TPGs that determine the complete transition coverage under any size constraint. It is shown that the testing of digital integrated circuits based on the LFSRs with primitive polynomials with large number of terms is better in the case of the two-test patterns. Based on the necessary and sufficient conditions, the two-test pattern testing is developed using the procedures outlined in this paper to get high robust path delay fault coverage with the optimal shortest test lengths.

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